1. A method of reducing boron segregation phenomena in an N channel, metal oxide semiconductor (NMOS) device via formation of a doped insulator region formed in an underlying insulator layer, comprising the steps of:

forming a semiconductor layer on an underlying insulator layer, wherein said insulator overlays a semiconductor substrate;

forming a hard mask layer on said semiconductor layer;

defining openings in said hard mask layer and in said semiconductor layer exposing a portion of said insulator layer and creating composite stacks comprised of hard mask shapes on semiconductor shapes;

laterally removing portions of said hard mask shapes exposing top portions of edges of said semiconductor shapes;

performing a ion implantation procedure to place ions in portions of said insulator layer exposed in said openings, and to place ions in portions of said insulator layer underlying portions of said semiconductor shapes;

performing an anneal procedure to activate said ions and forming said doped insulator region in portions of said insulator layer;

filling said openings with a second insulator layer; and

removing said hard mask shapes.

2. The method of claim 1, wherein said semiconductor layer is a silicon layer obtained at a thickness between about 10 to 1000 Angstroms, via SOI formation procedures.

3. The method of claim 1, wherein said insulator layer is comprised of silicon oxide formed at a thickness between about 50 to 5000 Angstroms.

4. The method of claim 1, wherein said hard mask layer is a silicon nitride layer, obtained via LPCVD or via PECVD procedures, at a thickness between about 100 to 1500 Angstroms.

5. The method of claim 1, wherein said openings in said hard mask layer and in said semiconductor layer are accomplished via an anisotropic RIE procedure.

6. The method of claim 1, wherein the width of said composite stacks comprised of hard mask shapes on semiconductor shapes, is between about 0.05 to 10 um.

7. The method of claim 1, wherein lateral pull back of said hard mask shapes, is accomplished via an isotropic wet etch procedure performed using H_3PO_4 or H_2PO_3 as an etchant for said hard mask shape.

8. The method of claim 1, wherein the length of lateral pull back of said hard mask shape is between about 10 to 500 Angstroms.

9. The method of claim 1, wherein said ion implantation procedure is performed using boron ions at an energy between about 1 to 10 KeV, at a dose between about 1E12 to 1E16 atoms/cm^2, and featuring an implantation angle between about 0 t 45 °.

10. The method of claim 1, wherein said ion implantation procedure is performed using nitrogen ions at an energy between about 1 to 10 KeV, at a dose between about 1E12 to 1E16 atoms/cm^2, and featuring an implantation angle between about 0 to 45 °.

11. The method of claim 1, wherein said anneal procedure is performed in hydrogen at a temperature between 800 to 1100° C, for a time between about 10 sec to 15 min, at a pressure between about 10 to 1000 torr.

12. The method of claim 1, wherein said doped insulator region is either a boron doped insulator region, a nitrogen doped insulator region, or a boron and nitrogen doped region.

13. The method of claim 1, wherein a nitrogen profile is located beneath that of a boron profile.

14. The method of claim 1, wherein said second insulator layer is a silicon oxide layer obtained via LPCVD, PECVD, HDPCVD, or SACVD procedures, at a thickness between about 100 to 5000 Angstroms.

15. A method of reducing a boron segregation phenomena in an N channel, metal oxide semiconductor (NMOS) device via formation of doped insulator regions in an underlying insulator layer, and via formation of a dielectric barrier layer surrounding insulator filled shallow trench shapes, comprising the steps of:

forming a silicon on insulator (SOI) layer wherein an insulator component of said SOI layer is comprised of silicon oxide, located on a semiconductor substrate;

forming a silicon nitride layer on said silicon layer;

performing an anisotropic dry etch procedures to form shallow trench isolation (STI) openings in said silicon nitride layer and in said silicon layer exposing a portion of said insulator layer, with unetched portions resulting in composite stacks comprised of silicon nitride shapes on silicon shapes;

performing an isotropic etch procedure to laterally remove portions of said silicon nitride shapes exposing edges of top portions of said silicon shapes;

performing a ion implantation procedure to place ions in portions of said insulator layer exposed in said STI openings, and to place ions in portions of said insulator layer underlying portions of said silicon shapes;

performing a hydrogen anneal procedure to activate said ions and to form said doped insulator region in portions of said insulator layer;

forming said dielectric barrier layer on exposed surfaces of said STI openings and on portions of said insulator layer exposed at bottom of said STI openings;

depositing a silicon oxide layer completely filling said STI openings;

performing a planarization procedure to form silicon oxide filled STI regions; and removing said silicon nitride shapes.

16. The method of claim 15, wherein said silicon layer of said SOI layer is obtained at a thickness between about 10 to 1000 Angstroms.

17. The method of claim 15, wherein said insulator component of said SOI layer is comprised of silicon oxide at a thickness between about 50 to 5000 Angstroms.

18. The method of claim 15, wherein said silicon nitride layer is obtained via LPCVD or via PECVD procedures, at a thickness between about 100 to 1500 Angstroms.

19. The method of claim 15, wherein said anisotropic dry etch procedure used to define STI openings in said silicon nitride layer and in said silicon layer is an anisotropic RIE procedure.

20. The method of claim 15, wherein the width of said composite stacks comprised of silicon nitride shapes on silicon shapes, is between about 0.05 to 10 um.

21. The method of claim 15, wherein said isotopic etch used to laterally remove portions of said silicon nitride shapes is an isotropic wet etch procedure performed using H_3PO_4 or H_2PO_3 as an etchant for silicon nitride.

22. The method of claim 15, wherein the length of lateral pull back of said silicon nitride shape is between about 10 to 500 Angstroms.

23. The method of claim 15, wherein said ion implantation procedure is performed using boron ions at an energy between about 1 to 10 KeV, at a dose between about 1E12 to 1E16 atoms/cm^2, and featuring an implantation angle between about 0 to 45 °.

24. The method of claim 15, wherein said ion implantation procedure is performed using nitrogen ions at an energy between about 1 to 10 KeV, at a dose between about 1E12 to 1E16 atoms/cm^2, and featuring an implantation angle between about 0 to 45 °.

25. The method of claim 15, wherein said anneal procedure is performed in hydrogen at a temperature between 800 to 1100° C, for a time between about 10 sec to 15 min, at a pressure between about 10 to 1000 torr.

26. The method of claim 15, wherein said doped insulator region is either a boron doped silicon oxide region, a nitrogen doped silicon oxide region, or a boron and nitrogen doped silicon oxide region.

27. The method of claim 15, wherein dielectric barrier layer is comprised of a nitrogen containing layer, at a thickness between about 10 to 1000 Angstroms.

28. The method of claim 15, wherein said dielectric barrier layer is a composite layer comprised of an overlying silicon nitride layer at a thickness between about 10 to 100 Angstroms, and of an underlying silicon oxide layer at a thickness between about 10 to 100 Angstroms.

29. The method of claim 15, wherein said silicon oxide layer used to fill said STI openings is obtained via LPCVD, PECVD, HDPCVD, or SACVD procedures at a thickness between about 100 to 5000 Angstroms.